TEXAS INSTRUMENTS

TLV5604/08/31 and TLV5614/10/30 Evaluation Module

User's Guide

October 2000

AAP Data Conversion

SLAU055

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TLV5604/08/10 (10 bit) and TLV5614/10/30 (12 bit) serial digital-to-analog converter evaluation module (EVM). A complete circuit description, as well as schematic diagram and bill of materials, is included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Overview
- Chapter 2 – Physical Description
- Chapter 3 – EVM Operation

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This is an example of a caution statement.

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Data Sheets:	**Literature Number:**
TLV5604	SLAS176A
TLV5614	SLAS188
TLV5610/08/29	SLAS268A
TLV5630/31/32	SLAS269A
TPS6734	SLVS127A
SN74AHC1G32	SCLS317H
SN74AHC1G08	SCLS314G
SN74AHC74	SCLS255G
SN74HC166	SCLS117B
SN74AHC32	SCLS247E
SN74AHC139	SCLS259H
SN74HC163	SCLS298
SN74AHC1G04	SCLS318I
Application Reports:	
TMS320C6000 EVM Daughterboard Interface	SPRA478

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Chapter 1

EVM Overview

This chapter gives a general overview of the TLV5604/08/31 and TLV5614/10/30 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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1.1 Features

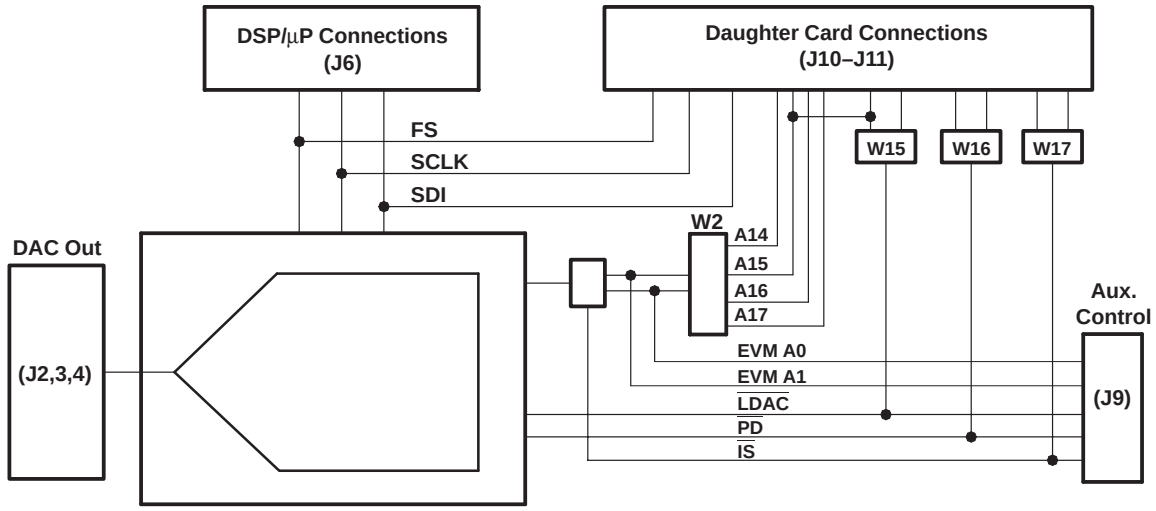
This EVM features three independent digital-to-analog converters on one convenient evaluation platform. The EVM is available in either a 10-bit or 12-bit version with the following devices installed:

EVM Version	Installed Devices	Number of DACs
10 Bit	TLV5604D	4
	TLV5608DW	8
	TLV5631DW	8
12 Bit	TLV5614D	4
	TLV5610DW	8
	TLV5630DW	8

The EVM contains a precision 5-V reference for the DACs, as well as connection terminals for an independent external reference. The analog outputs from each DAC are available on separate pin headers. Each DAC is address selectable through hardware or user supplied software. The EVM has a built-in test mode that allows the user to input a digital word to the DAC and verify the conversion result.

1.2 EVM Basic Functions

Figure 1–1. EVM Block Diagram



1.2.1 Standalone Testing

Closing W13 activates an onboard 20 MHz clock. This puts the EVM in self-test mode. The onboard oscillator provides the SCLK signal to the data converters and test circuitry.

Hardware jumpers W10, W12, and W14 allow the EVM user to select the DAC for evaluation. W10 and W12 control U3 and U4 respectively. Opening these

jumpers allows the frame sync signal to be routed to the data converter. W14 provides a chip select signal to U5 (pulls $\overline{CS}$ low). One, two, or all three DACs can be operated at the same time.

The onboard clock is fed through a 4-bit binary counter whose terminal count output is delayed one clock cycle and used as the DAC frame sync. In test mode, frame sync is common to all DACs. The test mode frame sync signal is inverted and used as the parallel-load enable signal to U10. This inverted signal also clears the binary counter (U9).

The two 8-channel data converters (U3 and U4) on this EVM support *daisy-chaining* of the serial input data. Jumpers W6 and W9 support the daisy chain devices. Jumper W11 allows the EVM user to configure the serial data source.

The EVM uses four banks of 4-bit switches to create a 16-bit serial word to the data converters. This is accomplished through the use of parallel-load serial shift registers U8 and U10. The internal configuration registers of the DACs can be set, and serial data can be simulated.

1.2.2 Testing With a Processor

When operated outside of the test mode (W13 open), the DACs expect to receive their control signals and serial data input from a host processor. The EVM works with TI's DSK series of digital signal processor evaluation boards that support the common connector interface described in *TMS320C6000 EVM Daughterboard Interface Application Report* (literature number SPRA478). Connectors J10 and J11, located on the underside of the EVM, provide the DSP interface.

Connectors J6, J7, and J8 allow the EVM user to define a custom processor interface. The shorting bars on J7 and J8 can be removed, allowing the EVM user to interface to older DSKs, micro controllers, or pattern generators.

1.2.2.1 EVM Address Bus

Address decoder U13 determines access to each data converter. A two-bit address bus on the EVM can be accessed via J9, or daughterboard connector J10. For TMS320C6000 systems using the common connector, jumper block W2 allows the user to select any two of the high order address bits A14, A15, A16 or A17.

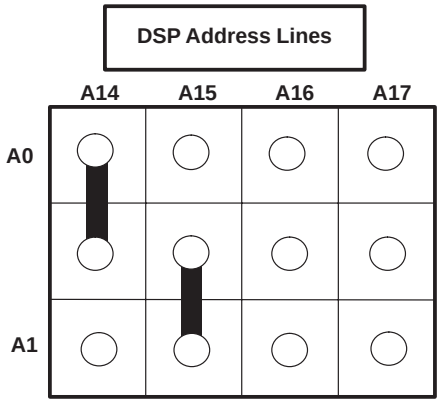
Note:

Address lines may vary depending on the DSP being used. Check your DSP EVM documentation for the specific address line mapping.

Jumper block W2 is configured as follows:

Note:

Rows A0 and A1 are common to the EVM address bus. The center row is connected to the DSP address bus via J10 pins 7 through 10. The following diagram shows the C6000 address lines A14 and A15 connected to EVM A0 and A1 respectively.



1.2.2.2 Address Function

Selection of the eight-channel DACs at U3 or U4 causes the frame sync and the serial data stream to be directed to the chosen device. Selection of the four-channel DAC at U5 puts a low-level signal on its chip select pin.

Address	Function
00	No selection made (default)
01	Selects U3 to receive frame sync
10	Selects U4 to receive frame sync
11	Selects U5 to receive chip select (active low signal)

1.3 Power Requirements

1.3.1 Supply Voltage

The DAC EVM is designed to operate from 3.3 V to 5.5 V. The EVM requires 170 mA at 3.3 V and 150 mA at 5.5 V. Power to the EVM can be applied via J1 from an external supply, or can be directed through the common connector interface via J10. Jumper W1 allows the EVM user to select either the 3.3-V or 5-V bus from the DSP.

CAUTION

When using an external power supply via J1, remove jumper W1 to avoid potential damage to the DSP circuitry.

1.3.2 Reference Voltage

TP5 and TP6 allow the use of an external DAC reference source. An external reference of not more than 5 Vdc can be applied to TP6 referenced to TP5.

Variable resisters R3, R4, and R36 can be used to adjust the reference voltages to U3, U5, and U4 respectively. Jumper W3 allows the EVM user to switch between the EVM reference circuit and the external reference source.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM, and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a four-layer printed circuit board using FR-4 material. Dimensions are 134,6 mm (5.30 inch) × 86 mm (3.39 inch) × 1,57 mm (0.062 inch) thick. Figures 2–1 through 2–5 show the assembly and individual artwork layers.

Figure 2–1. Top Assembly

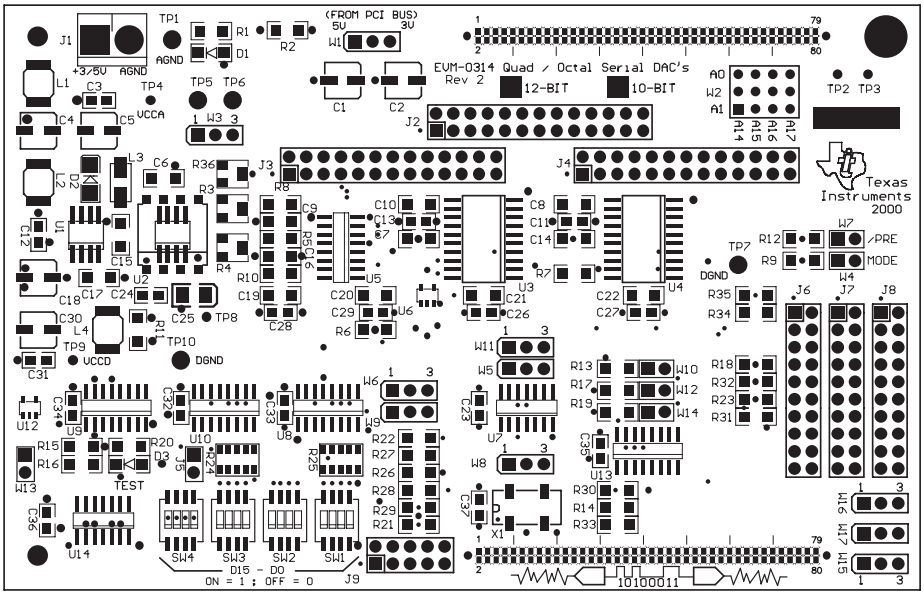


Figure 2–2. Layer 1

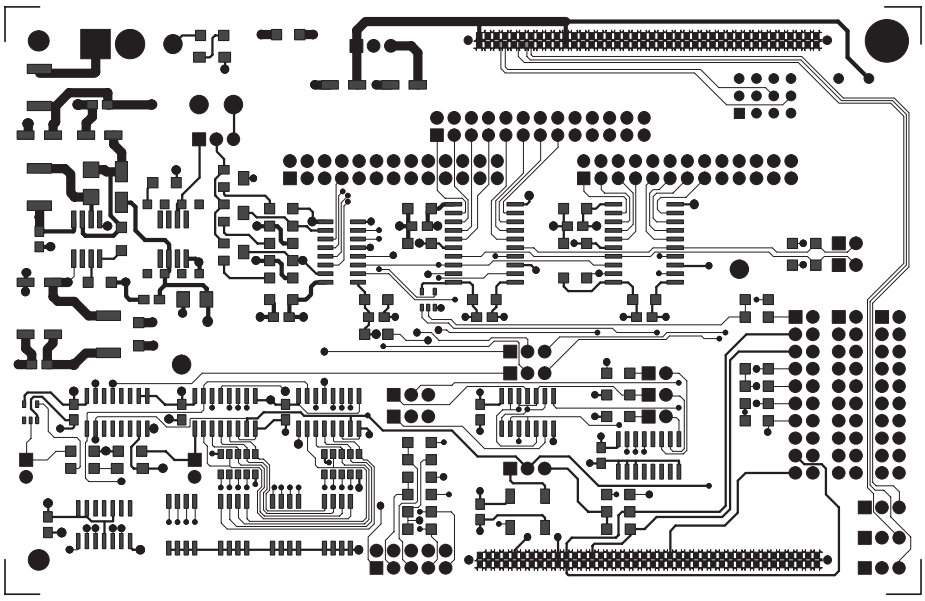


Figure 2–3. Layer 2

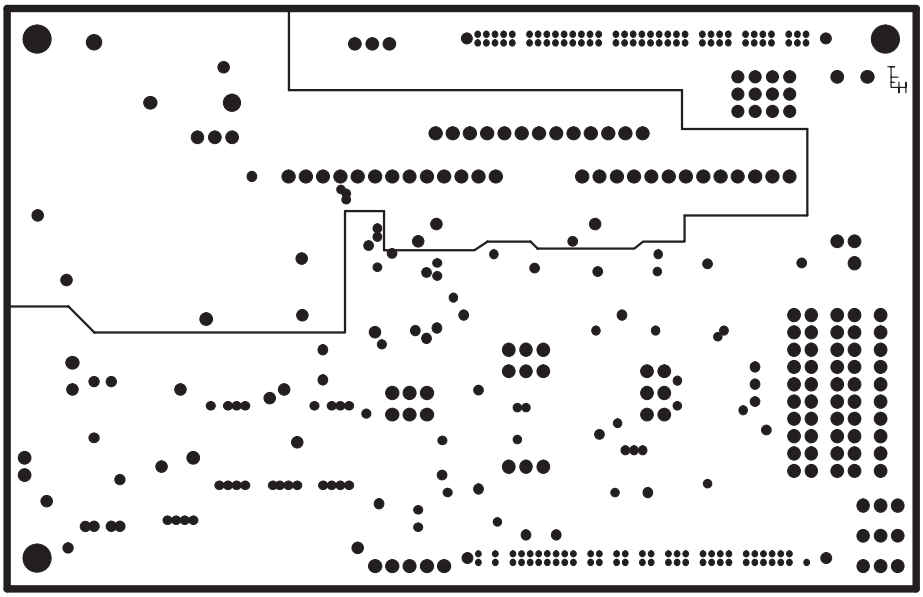


Figure 2–4. Layer 3

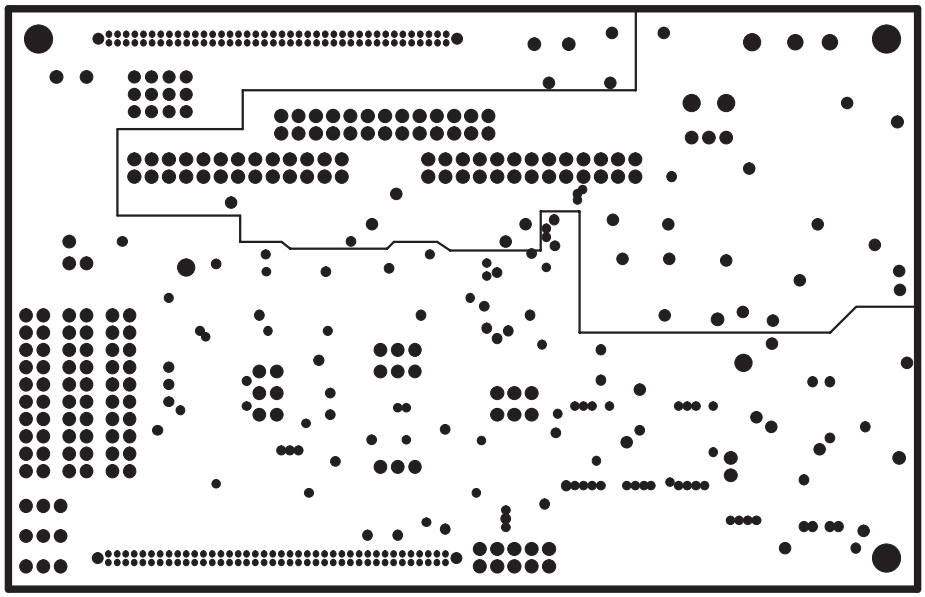
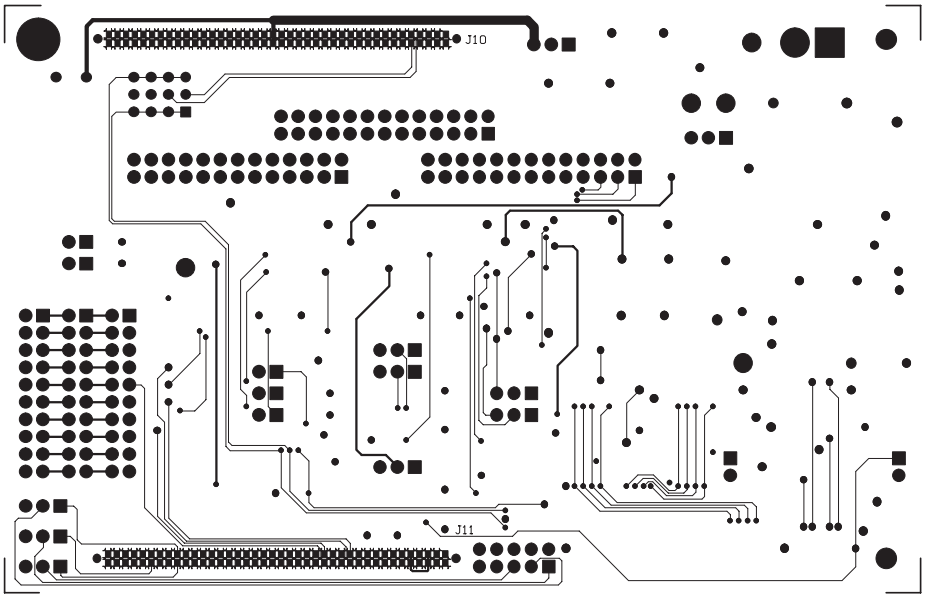


Figure 2–5. Layer 4



2.2 Parts List

Item No.	Qty		Reference Des.	Value	Manufacturer/ Distributor	Part Number
	10 Bit	12 Bit				
1	1	1	0315R2EVM PCB	NA		
2	2	2	C1 C2	10 µF	Panasonic	ECEV1CA100SR
3	17	17	C3 C11 C12 C13 C23 C24 C26 C27 C28 C29 C31 C32 C33 C34 C35 C36 C37	0.1 µF	Panasonic	ECJ–2YB1H103K
4	4	4	C4 C5 C18 C30	33 µF	Panasonic	ECEV1AA330SR
5	2	2	C6 C15	1 nF	Panasonic	ECU–V1H102JCH
6	11	11	C7 C8 C9 C10 C14 C16 C17 C19 C20 C21 C22	0.01 µF	Panasonic	ECU–V1H103JCH
7	1	1	C25	10 µF	Panasonic	ECSH1CC106R
8	1	1	D1	GREEN	Chicago Miniature	CMD15–21VGC/TR8
9	1	1	D2	1N5817	Diodes, Inc.	1N5817M
10	1	1	D3	AMBER	Chicago Miniature	CMD15–21VYC/TR8
11	1	1	J1	KRMZ2	Lumberg	KRMZ2
12	3	3	J2 J3 J4	26PIN_IDC	Samtec	TWS–113–07–L–D
13	3	3	J6 J7 J8	20PIN_IDC	Samtec	TWS–110–07–L–D
14	1	1	J9	10PIN_IDC	Samtec	TWS–105–07–L–D
15	2	2	J10 J11	TFM–140	Samtec	TFM–140–31–S–D–A
16	2	2	L1 L4	4.7 µH	Inductor Warehouse	CTDO1608C–472
17	1	1	L2	15 µH	Inductor Warehouse	CTDO1608C–153
18	1	1	L3		FAIR-RITE	2744044447
19	4	4	R1 R15 R16 R20	1K	Panasonic	ERJ–8GEYJ102V

Item No.	Qty		Reference Des.	Value	Manufacturer/ Distributor	Part Number
	10 Bit	12 Bit				
20	2	2	R2 R11	0 Ω	Panasonic	ERJ–8GEYJ00V
21	3	3	R3 R4 R36	10K	Bourns	3214W–1–103E
22	3	3	R5 R8 R10	2.5K	Panasonic	ERJ–8GEYJ252V
23	13	13	R6 R7 R9 R12 R13 R17 R19 R21 R26 R27 R29 R30 R35	10K	Panasonic	ERJ–8GEYJ103V
24	9	9	R14 R18 R22 R23 R28 R31 R32 R33 R34	33	Panasonic	ERJ–8GEYJ330V
25	2	2	R24 R25	10K	CTS Corp	745C101103JTR
26	4	4	SW1 SW2 SW3 SW4	SPST	C&K	TD04H0SK1
27	5	5	TP1 TP5 TP6 TP7 TP10	TP_TURRENT	Cambion	180–7337–02–05
28	6	6	TP2 TP3 TP4 TP8 TP9 TP11	TP_.025	Keystone Electronics	5000K–ND
29	1	1	U1	TPS6734ID	Texas Instruments	TPS6734ID
30	1	1	U2	5.0 V Ref.	Burr-Brown/ Thaler Corporation	REF02BU/VRE3050A
31	1		U3	TLV5631DW	Texas Instruments	TLV5631DW
32	1		U4	TLV5608DW	Texas Instruments	TLV5608DW
33	1		U5	TLV5604D	Texas Instruments	TLV5604D
34		1	U3	TLV5630DW	Texas Instruments	TLV5630DW
35		1	U4	TLV5610DW	Texas Instruments	TLV5610DW
36		1	U5	TLV5614D	Texas Instruments	TLV5614D
37			U6	SN74AHC1G32	Texas Instruments	SN74AHC1G32DBV
38	1	1	U7	SN74AHC32	Texas Instruments	SN74AHC32D
39	2	2	U8 U10	SN74HC166	Texas Instruments	SN74HC166D
40	1	1	U9	SN74HC163	Texas Instruments	SN74HC163D
41	2	2	U11 U12	SN74AHC1G04	Texas Instruments	SN74AHC1G04DBVR
42	1	1	U13	SN74AHC139	Texas Instruments	SN74AHC139D
43	1	1	U14	SN74AHC74	Texas Instruments	SN74AHC74D
44	11	11	W1 W3 W5 W6 W8 W9 W11 W15 W16 W17	3 Pin Jumper	Samtec	TSW–103–07–LS
45	1	1	W2	3X4X.1	Samtec	TSW–104–07–LT
46	7	7	J5 W4 W7 W10 W12 W13 W14	2 Pin Jumper	Samtec	TSW–102–07–LS
47	1	1	X1	20MHz	Epson	SG–8002JC20.0M–PHBS

Chapter 3

EVM Operation

The EVM is factory tested and configured for immediate operation with a few simple connections.

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3.1 Standalone Testing

Connect a positive DC source of 3.3 to 5 volts to the EVM at connector J1–1 referenced to J1–2. LED indicators D1 and D3 should illuminate, indicating that power is applied to the board, and the EVM is in test mode.

3.1.1 Test Mode—Factory Defaults

Jumpers W10, W12, and W14 are open. This allows the serial data and frame sync signals to be directed to each data converter. Frame sync is automatically generated and occurs every sixteenth clock cycle. Trim potentiometers R3 and R4 are set to provide U3 and U5 with 2.048V, while trim potentiometer R36 provides U4 with 4.096 V.

Switch banks SW1 through SW4 are located along the bottom edge of the EVM. These switches are factory set to provide the digital-to-analog converters with hex word 0x0800. This word translates to half-scale output on channel 0 of each converter, and can be seen on pin 1 of connectors J3 (U5), J2 (U3), and J4 (U4).

3.1.2 Test Mode—TLV5604/14

Closing jumpers W10 and W12 allows independent testing of the four-channel data converter at U5.

Switch bank SW4 is used for channel selection, power down, and conversion speed. Selection of channels 0 through 4 requires the setting/clearing of bits D15 and D14. Setting bit D13 will put the data converter in power-down mode. Setting bit D12 will choose fast conversion mode. Switch banks SW3, SW2, and SW1 provide the digital input to the converter.

TLV5604/14 Register Configuration:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A0	A1	PWR	SPD	DAC Value											

Channel Selection:

A1	A0	DAC/Output Connector
0	0	OUT A / J3–1
0	1	OUT B / J3–3
1	0	OUT C / J3–5
1	1	OUT D / J3–7

Power and Speed Selection:

D13 – PWR	D12 – SPD	Function
0	X	Normal Operation
1	X	Power Down Mode
X	0	Slow conversion mode
X	1	Fast conversion mode

DAC Output Value:
Vout = 2Vref CODE/0x1000

Data bits D11 through D0 set the digital input value to be converted. Each bit can be set independently by sliding the appropriate switch to the on position (towards the middle of the EVM). Data is presented to the converter MSB first. On the 10-bit TLV5604, data in locations D1 and D0 are ignored.

3.1.3 Test Mode—TLV5610/08

Jumper W12 controls the eight-channel DAC at U4. This data converter can be tested alone or in daisy chain mode with U3.

Switch bank SW4 serves two functions for these devices. During DAC write cycles, SW4 selects the control register to be accessed. DAC write cycles are initiated by setting bit D15.

TLV5610/08 Configuration Register 0:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	X	X	X	X	X	X	X	PD	DO	X	X	IM

PD: Full device power down — 0 = Normal; 1 = Power Down
DO: Digital output enable — 0 = Disable; 1 = Enable
IM: Input Mode — 0 = Binary; 1 = 2s Complement
X: Reserved

TLV5610/08 Configuration Register 1:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	X	X	X	X	P_{GH}	P_{EF}	P_{CD}	P_{AB}	S_{GH}	S_{EF}	S_{CD}	S_{AB}

P_{XY}: Power down DAC_{XY} — 0 = Normal; 1 = Power Down
S_{xy}: Speed DAC_{XY} — 0 = Slow 1 = Fast
XY: DAC Pair AB, CD, EF, GH

During DAC read cycles, SW4 selects the output channel to be updated. DAC read cycles are initiated by clearing bit D15.

TLV5610/08 Data Register:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	DAC Value											

Channel Selection:

A3	A2	A1	A0	DAC/Output Connector
0	0	0	0	OUT A / J4–1
0	0	0	1	OUT B / J4–3
0	0	1	0	OUT C / J4–5
0	0	1	1	OUT D / J4–7
0	1	0	0	OUT E / J4–9
0	1	0	1	OUT F / J4–11
0	1	1	0	OUT G / J4–13
0	1	1	1	OUT H / J4–15

DAC Output Value:
Vout = Vref CODE/0x1000

Data bits D12 through D0 set the digital input value to be converted. Each bit can be set independently by sliding the appropriate switch to the on position (towards the middle of the EVM). Data is presented to the converter MSB first. On the 10-bit TLV5608, data in locations D1 and D0 are ignored.

3.1.4 Test Mode—TLV5630/31

Jumper W10 controls the eight-channel DAC at U3. This data converter can be tested alone or in daisy chain mode with U4.

Switch bank SW4 serves two functions for these devices. During DAC write cycles, SW4 selects the control register to be accessed. DAC write cycles are initiated by setting bit D15.

TLV5630/31 Configuration Register 0:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	X	X	X	X	X	X	X	PD	DO	R1	R0	IM

PD: Full device power down — 0 = Normal; 1 = Power Down
DO: Digital output enable — 0 = Disable; 1 = Enable
R1/R0: Reference Select — 00 = Ext., 01 = Ext., 10 = Int. 1 V, 11 = Int. 2 V
IM: Input Mode — 0 = Binary; 1 = 2s Complement
X: Reserved

TLV5630/31 Configuration Register 1:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	X	X	X	X	P_{GH}	P_{EF}	P_{CD}	P_{AB}	S_{GH}	S_{EF}	S_{CD}	S_{AB}

P_{XY}: Power down DAC_{XY} — 0 = Normal; 1 = Power Down
S_{xy}: Speed DAC_{XY} — 0 = Slow 1 = Fast
XY: DAC Pair AB, CD, EF, GH

During DAC read cycles, SW4 selects the output channel to be updated. DAC read cycles are initiated by clearing bit D15.

TLV5610/08 Data Register:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	DAC Value											

Channel Selection:

A3	A2	A1	A0	DAC/Output Connector
0	0	0	0	OUT A / J2–1
0	0	0	1	OUT B / J2–3
0	0	1	0	OUT C / J2–5
0	0	1	1	OUT D / J2–7
0	1	0	0	OUT E / J2–9
0	1	0	1	OUT F / J2–11
0	1	1	0	OUT G / J2–13
0	1	1	1	OUT H / J2–15

DAC Output Value:
Vout = 2Vref CODE/0x1000

Data bits D12 through D0 set the digital input code to be converted. Each bit can be set independently by sliding the appropriate switch to the on position (towards the middle of the EVM). Data is presented to the converter MSB first. On the 10-bit TLV5631, data in locations D1 and D0 are ignored.

3.2 Processor Controlled Testing

This section describes the operation of the EVM through a host processor such as a DSP or microcontroller. Daughterboard connectors J10 and J11 are designed for direct plug in to a DSP development board. Connectors J6 through J9 however, can be used to develop a custom interface to suit most any situation. Each of the following subsections gives the EVM user the necessary information required to successfully operate the data converters.

3.2.1 Address Selection

When testing the EVM with a host processor, several options are available. Closing jumpers W10, W12, and W14 allow the user to access the data converters via address decoder U13. Address selecting U3 or U4 allows the serial input data and frame sync signals to be applied to the selected device.

EVM Address Bus:

A1– J9.9	A0 – J9.7	Reference	Selection Results	Device
0	0	N/A	None	None
0	1	U3	SDI + FS	TLV5630 / TLV5631
1	0	U4	SDI + FS	TLV5610 / TLV5608
1	1	U5	$\overline{CS}$	TLV5604 / TLV5614

The output enable pin for the address decoder can be controlled through the DSP interface via W17. When W17 is in position 1-2 the $\overline{IS}$ signal of the DSP is used to enable the decoder. Position 2-3 uses the DSP address line DC_A15. The output enable pin can also be tied low by inserting a shorting jumper across J9 pins 1-2.

3.2.2 Frame Sync

When using this EVM with a host processor, jumper W5 must be moved to position 2-3. This allows an external frame sync signal to be applied to the data converters via J11-23 or J6-11. This external frame sync signal is directed to the eight-channel data converters based on the state of the address bus.

The TLV5604/14 device located at position U5 will receive a frame sync and serial input data regardless of the state of the address bus. This device uses a dedicated chip-select pin to control conversion. The frame sync and serial data inputs are ignored while chip select is high.

3.2.3 Serial Input Data

When using this EVM with a host processor, jumper W11 must be moved to position 2-3. This allows serial input data from the host processor to be applied to the selected data converter via J11-24 or J6-7.

U3 and U4 have the ability to work in *daisy-chain* fashion. When DOUT is enabled in either device, jumpers W6 and W9 can select the source of the serial input data. The data is buffered and then shifted via the DOUT pin (U3 or U4, pin 19) after a 16-clock cycle delay.

3.2.4 Serial Clock

When the serial clock is supplied from an external host, jumper W18 must be in position 2-3. The serial clock can be supplied via the common connector interface at J11-21 or J6-3. Check the appropriate device data sheet for maximum serial clock specifications.

3.2.5 Load DAC

The *load DAC* (/LDAC) pin is designed to simultaneously update all of the DAC outputs with the current conversion data. This is an asynchronous pin that can be held low permanently, if simultaneous updates are not required. This pin is held at a low state by default on the EVM via pulldown resistor R27. This signal can be controlled through J9-5. DSP users can select to control /LDAC from either DC_A13 at J10-13 or DC_CNTL0 at J11-64 through jumper W15.

3.2.6 MODE

Jumper W4 controls the signal level on the mode pin of U3 and U4. When operated in DSP mode, W4 should be closed (MODE = 0). This causes the DAC outputs to update after the 16^{th} falling clock edge.

Opening W4 causes U3 and U4 to operate in microprocessor mode (MODE = 1). In this condition, frame sync must be asserted high after the 16^{th} falling clock edge, or the conversion will be lost.

3.2.7 Power Down

The four-channel device at U5 has a power-down pin that can be accessed from J9-3. A low level on this pin will send the device into power-down mode. DSP users can select either DC_CNTRL1 at J11-63 or DC_A12 via W16 as the source of this control.

3.3 Jumper Settings

The following table shows the function of each jumper on the EVM:

Reference	Setting	Function
W1	Pin 1-2 Closed	Provides EVM with 5 V from the DSP
	Pin 2-3 Closed	Provides EVM with 3.3 V from the DSP
W2	See Section 1.2	Provides DSP to EVM address mapping
W3	Pin 1-2 Closed	Provides DACs with onboard reference
	Pin 2-3 Closed	Allows DACs to use external reference via TP6
W4	Open	Puts U3 and U4 in microprocessor mode
	Closed	Puts U3 and U4 in DSP mode
W5	Pin 1-2 Closed	Applies test mode frame sync to data converters
	Pin 2-3 Closed	Applies host processor frame sync to data converters
W6	Pin 1-2 Closed	Supplies U4 with Serial Data Input signal
	Pin 2-3 Closed	Supplies U4 with DOUT signal from U3
W7	Open	Puts low level signal on U3 / U4 Preset pins
	Closed	Puts high level signal on U3 / U4 Preset pins
W8	Pin 1-2 Closed	Supply data converters with test mode serial clock
	Pin 2-3 Closed	Supply data converters with host mode serial clock
W9	Pin 1-2 Closed	Supplies U3 with Serial Data Input signal
	Pin 2-3 Closed	Supplies U3 with DOUT signal from U4
W10	Open	Bypasses address selection for U3
	Closed	Sets U3 to EVM address 01
W11	Pin 1-2 Closed	Supplies test mode SDI to DACs
	Pin 2-3 Closed	Supplies host mode SDI to DACs
W12	Open	Bypasses address selection for U4
	Closed	Sets U4 to EVM address 10
W13	Open	Puts the EVM in Host mode
	Closed	Puts the EVM in Test Mode
W14	Open	Bypasses address selection for U5
	Closed	Sets U5 to EVM address 11
W15	Pin 1-2 Closed	Allows DSP users to select DC_CNTL0 as $\overline{\text{LDAC}}$ control
	Pin 2-3 Closed	Allows DSP users to select DC_A13 as $\overline{\text{LDAC}}$ control
W16	Pin 1-2 Closed	Allows DSP users to select DC_CNTL1 as $\overline{\text{PD}}$ control
	Pin 2-3 Closed	Allows DSP users to select DC_A12 as $\overline{\text{PD}}$ control
W17	Pin 1-2 Closed	Allows DSP users to select DC_$\overline{\text{IS}}$ as address decoder enable
	Pin 2-3 Closed	Allows DSP users to select DC_A15 as address decoder enable

3.4 I/O Connector Signals

The following tables show the signal pins available to the EVM from the input/output connectors.

Daughterboard Connector J10 (unused pins omitted for clarity):

Signal	Pin	Pin	Signal
+5 V	1	2	+5 V
DC_A17	7	8	DC_A16
DC_A15	9	10	DC_A14
Ground	11	12	Ground
DC_A13	13	14	DC_A12
+5 V	21	22	+5 V
Ground	31	32	Ground
+3.3 V	41	42	+3.3 V
Ground	51	52	Ground
Ground	61	62	Ground
Ground	71	72	Ground
Ground	79	80	Ground

Daughterboard connector J11 (unused pins omitted for clarity):

Signal	Pin	Pin	Signal
Ground	3	4	Ground
+5 V	5	6	+5 V
Ground	7	8	Ground
+5 V	9	10	+5 V
+3.3 V	19	20	+3.3 V
CLKX	21	22	CLKS
FSX	23	24	DX
Ground	25	26	Ground
CLKR	27	30	DR
FSR	29	32	Ground
Ground	31	38	Ground
Ground	37	44	Ground
Ground	43	52	Ground
TOUT	45	62	Ground
XF	49	64	DC_CNTL0
Ground	51	70	DC_$\overline{IS}$
Ground	61	76	Ground
DC_CNTL1	63	80	Ground
Ground	75		
Ground	77		
Ground	79		

DSP/Micro Connector J6:

Signal	Pin	Pin	Signal
$\overline{XF}$	1	2	DGND
CLKX	3	4	DGND
CLKR	5	6	DGND
DX	7	8	DGND
DR	9	10	DGND
FSX	11	12	DGND
FSR	13	14	DGND
SPARE	15	16	DGND
CLKS	17	18	DGND
TOUT	19	20	DGND

DSP/Micro Connector J9:

Signal	Pin	Pin	Signal
$\overline{IS}$	1	2	DGND
$\overline{PD}$	3	4	DGND
$\overline{LDAC}$	5	6	DGND
EVM A1	7	8	DGND
EVM A0	9	10	DGND

3.5 DAC Output Connectors

The following tables show the signal pins of the data converter output connectors:

U3 (TLV5630/TLV5631) Data Converter Output J2:

Signal	Pin	Pin	Signal
DAC_A	1	2	AGND
DAC_B	3	4	AGND
DAC_C	5	6	AGND
DAC_D	7	8	AGND
DAC_E	9	10	AGND
DAC_F	11	12	AGND
DAC_G	13	14	AGND
DAC_H	15	16	AGND
SPARE	17–25	18–26	AGND

U4 (TLV5610/TLV5608) Data Converter Output J4:

Signal	Pin	Pin	Signal
DAC_A	1	2	AGND
DAC_B	3	4	AGND
DAC_C	5	6	AGND
DAC_D	7	8	AGND
DAC_E	9	10	AGND
DAC_F	11	12	AGND
DAC_G	13	14	AGND
DAC_H	15	16	AGND
SPARE	17–25	18–26	AGND

U5 (TLV5614/TLV5604) Data Converter Output J3:

Signal	Pin	Pin	Signal
DAC_A	1	2	AGND
DAC_B	3	4	AGND
DAC_C	5	6	AGND
DAC_D	7	8	AGND
SPARE	9–25	18–26	AGND

3.6 Schematic Diagrams

The following pages show a complete schematic diagram of the evaluation module.

Revision History		
REV	ECN Number	Approved

W13
(Close for test mode)
TEST
VCCD
X1
VCC
OE
GND
OUT
20MHz
C37
0.1uF
U12
SN74HC1G04
R15
10K
R16
1K
D3
AMBER
TEST
W8
SCLK
EXT_CLK

U9
SN74HC163
CLR
LOAD
ENT
ENP
CLK
A
B
C
D
RCO
QA
QB
QC
QD
U14A
SN74AHC74
PRE
CLK
D
CLR
Q
C36
0.1uF
EXT_FS
W5
FS

U7A
SN74AHC32
FS
AD_01
U7B
SDI
R7
10K
DOUT2
W9
U7C
AD_10
R6
10K
DOUT1
W6
U7D

U3
TLV5630/31DW
SCLK
FS
/LDAC
MODE
/PRE
DIN
DOUT
DVdd
DGND
OUT_A
OUT_B
OUT_C
OUT_D
OUT_E
OUT_F
OUT_G
OUT_H
AVdd
REF
AGND
C26
0.1uF
C21
0.01uF
VCCA
VREF1
C7
0.01uF
C10
0.01uF
C13
0.1uF
J2

U4
TLV5610/08DW
C27
0.1uF
C22
0.01uF
VREF3
C14
0.01uF
C8
0.01uF
C11
0.1uF
J4

U5
TLV5614/04D
/CS
REF_AB
REF_CD
C29
0.1uF
C20
0.01uF
VREF2
C9
0.01uF
C16
0.01uF
C19
0.01uF
C28
0.1uF
J3

J5
R20
1K
U10
SN74HC166M
SDI_D0
SDI_D1
SDI_D2
SDI_D3
SDI_D4
SDI_D5
SDI_D6
SDI_D7
DS
D0
D1
D2
D3
D4
D5
D6
D7
MR
PE
CE
CP
Q7
C32
0.1uF
U8
SN74HC166M
SDI_D8
SDI_D9
SDI_D10
SDI_D11
SDI_D12
SDI_D13
SDI_D14
SDI_D15
C33
0.1uF
EXT_SDI
W11
SDI

U13B
SN74HC139
A0
A1
/IS
A
B
G
Y0
Y1
Y2
Y3
W10
W12
W14
AD_01
AD_10
AD_11
R19
10K
R17
10K
R13
10K

CONTROL
CLKX
DX
FSX
FSR
DR
CLKR
/XF
/PD
/LDAC
MODE
/PRE
R14
R18
R23
R31
R32
R33
R34
R28
R22
33
EXT_CLK
EXT_SDI
EXT_FS
/PD
/LDAC
MODE
/PRE

U6
SN74HC1G32
AD_11
R35
10K

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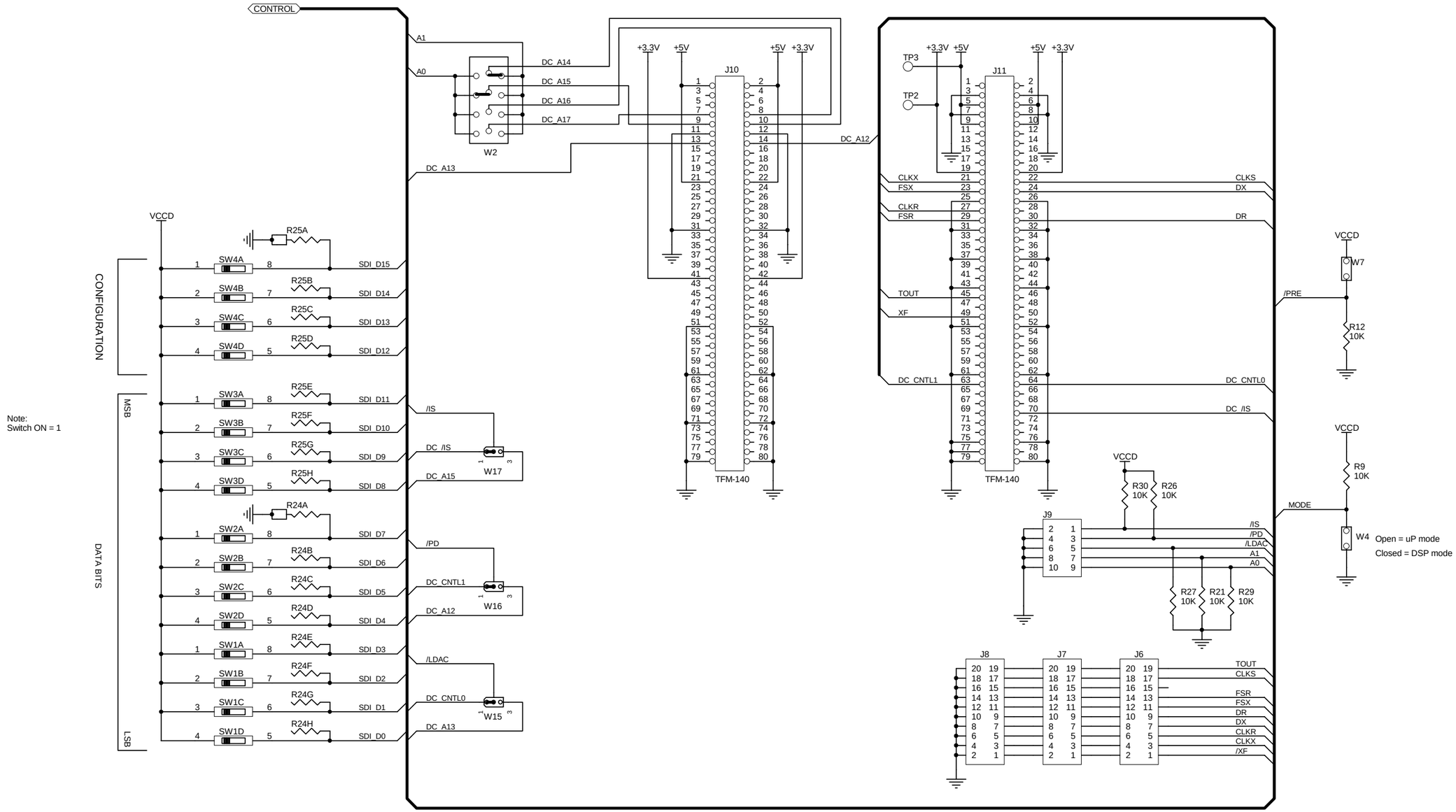
Title: Quad / Octal Serial DAC EVM Schematic			
Engineer:			
Drawn By: T. Hendrick	SIZE:	DATE: 22-Sep-2000	REV: 2
FILE: EVM_0314.DDB			SHEET: 1 OF: 3

TMS320 Common Connector Interface



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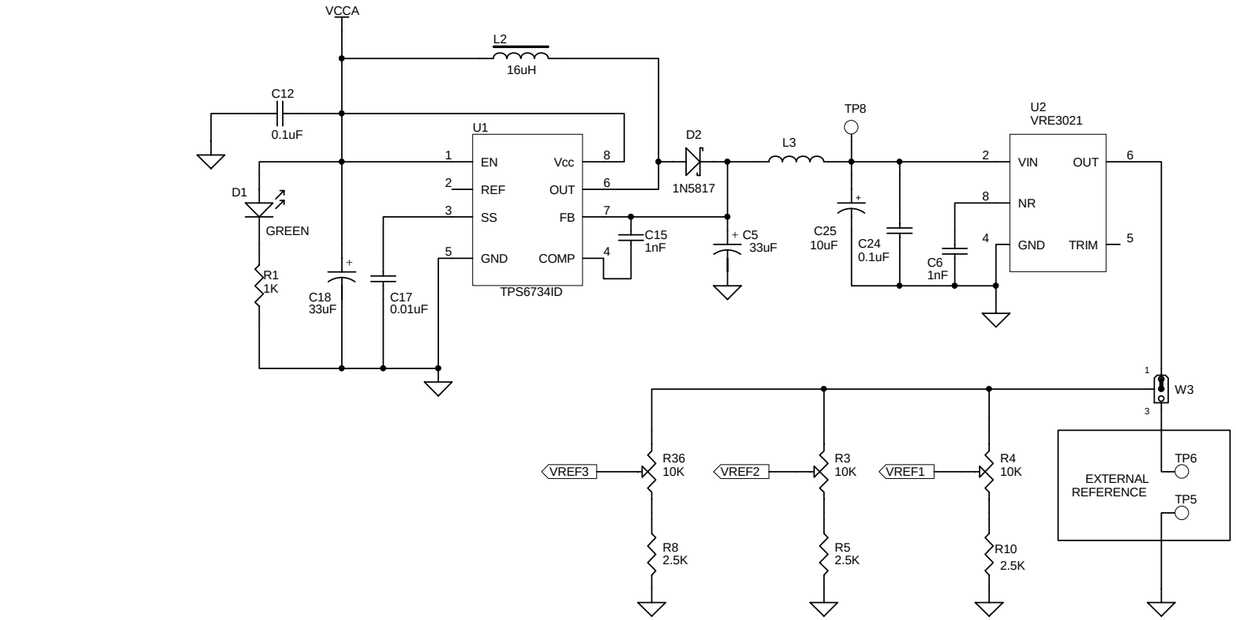

12500 TI Boulevard. Dallas, Texas 75243	
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Drawn By: T. Hendrick	SIZE: DATE: 22-Sep-2000 REV: 2
FILE: EVM_0314.DDB	SHEET: 3 OF: 3